The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A method of conducting a behavioral simulation of one or more process blocks in an electronic design, the method comprising:

receiving an assignment decision diagram representation of the process block and including one or more control nodes for maintaining control flow through the simulator, thereby creating one or more break points; and

running a simulation of the assignment decision diagram representation, whereby the simulation may be stopped when control nodes are encountered so that the state of the simulation may be observed.

2. (Original) A method as recited in claim 1, wherein the assignment decision diagram representation comprises:

an assignment value portion representing the computation of values that are to be assigned to a storage unit of an output port, wherein the values are computed from current contents of storage units, input ports, or constants provided to the ADD;

an assignment condition portion connected as a data flow path representing the computation of a particular condition such that the end product of the condition computation is a binary value that evaluates to either *TRUE* or *FALSE*;

an assignment decision node (ADN) that selects a value from a set of input values computed by the assignment value portion based upon the conditions computed by the assignment condition portion; and

an assignment target portion that is provided with the selected value from the corresponding ADN corresponding to the true ADN condition.

3. (Original) A method as recited in claim 1, wherein the control node is selected from the group comprising a query control node used to represent a conditional branch in a control flow, an evaluation/assignment control node used to represent an assignment operation, a null control node used as a place holder, and a suspend control node used to suspend execution of the process block.

4. (Original) A method as recited in claim 3, wherein the suspend control node is selected from the group comprising an event type suspend control node used to suspend execution of the process block pending a pre-determined future event and a delay type suspend control node used to suspend execution of the process block for a for a specific length of time.

5. (Original) A method as recited in claim 4, wherein the control node includes a control node pointer that is used to point to the portion of the assignment decision diagram representation being simulated.

6. (Original) A method as recited in claim 5, wherein the running a simulation of the assignment decision diagram representation comprises:

simulating a first portion of the assignment decision diagram that is associated with a first control node, the first control node having a first control node pointer that points to the first portion of the assignment decision diagram during simulation; and

simulating a second portion of the assignment decision diagram that is associated with a second control node that is different from the first control node, the second control node having a second control node pointer that points to the second portion of the assignment decision diagram during simulation, wherein the simulator traverses the control nodes associated with the

assignment decision diagram representation starting at the first control node and ending at a last control node representing the end of the assignment decision diagram representation.

7. (Currently Amended) A method as recited in claim 6, wherein one or more break points are created by stopping the simulation at a selected control node**[s]** such that the simulation is paused at those portions of the assignment decision diagram representation corresponding to the paused control nodes.

8. (Original) A behavioral simulator for conducting a behavioral simulation of one or more process blocks in an electronic design, the behavioral simulator comprising:

one or more processors;

memory coupled to at least one of the one more processors; and

a display coupled to at least one of the one or more processors to display simulation results, wherein the processor is configured or designed to run a simulation of an assignment decision representation of the process block and stop the simulation when encountering control nodes in the assignment decision representation so that the state of the simulation can be observed.

9. (Original) A behavioral simulator as recited in claim 8, wherein the display comprises:

an input data portion arranged to display selected input data representing the one or more process blocks in the electronic design;

a process block status portion arranged to display the status of selected process blocks;

a process block portion arranged to display process statements included in the process block being simulated; and

a process block variable portion arranged to display those variables to be viewed while the simulation of the process block is paused.

10. (Original) A behavioral simulator as recited in claim 9, wherein the process block portion comprises:

one or more process statements;

a process statement highlighter used to highlight the process statement being simulated; and

a process statement flag used to indicate the process statement being paused.

11. (Original) A behavioral simulator as recited in claim 10, wherein the variables viewed in the process block variable portion are associated with the paused process statement.

12. (Original) A behavioral simulator as recited in claim 11, wherein the display is a graphical user interface.